Plasma Apparatus and Meth d Capable f Adaptive Impedance Matching

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an apparatus of the fabrication of integrated circuits, and the present invention especially relates to an apparatus of the fabrication of integrated circuits which is capable of reducing gate oxide damage in a high density plasma chemical vapor deposition process to which a bi-polar electrostatic chuck is applied.

2. Description of the Prior Art

After the fabrication of the active device of a MOS(metal-oxide semiconductor) device is accomplished, the following work is to proceed the fabrication of the multilevel interconnects above the MOS device. As the process technology progresses and scales of MOS devices get more and more smaller, gaps between metal conductors also become more and more narrower. Accordingly, gaps of high aspect ratio between metal conductors are formed. The gaps of high aspect ration will let the deposition of dielectric layers become incomplete and form voids in the dielectric layers. These voids in the dielectric layers will damage electric properties of MOS devices and lead to scraped wafers.

In order to solve the problem of the incomplete deposition of dielectric layers, a HDPCVD(high density plasma chemical vapor

deposition) process is proposed to deposit dielectric layers between metal conductors in U.S Pat. No. 6,239,018 and U.S Pat. No. 6,218,284. The detailed description of a HDPCVD process is also contained in U.S Pat. No. 6,117,345. The main reason a HDPCVD process can solve the problem of the incomplete deposition of dielectric layers is that a HDPCVD process is capable of both proceeding chemical vapor deposition process and anisotropic etching process. As shown in FIG.1A, the etching function results from the following steps: an AC(alternating current) plasma generating source 12 of the HDPCVD equipment 10 generates plasma 16, the voltage potential difference between the plasma 16 and the electrostatic chuck 20 attracts the ions of the plasma 16 to bombard the wafer 18. The ions of the plasma 16 will anisotropically etch the excess dielectric layers above the metal conductors of MOS devices to deposit void-free dielectric layers. Because the voltage potential difference between the plasma 16 and the electrostatic chuck 20 distributes non-uniformly in the process of ion-bombardment on the wafer 18, currents are produced on the wafer 18 surface. If the voltage potential difference between the plasma 16 and the electrostatic chuck 20 distributes extremely non-uniformly, the produced currents will damage gate oxides of MOS devices.

The non-uniform distribution of the voltage potential difference between the plasma 16 and the electrostatic chuck 20 possibly results from the non-uniform distribution of the voltage potential on the electrostatic chuck 20. In HDPCVD equipment, the type of an electrostatic chuck 20 includes mono-polar and bi-polar. The electrostatic chuck 20 secures the wafer 18 by means of the electrostatic force. If the electrostatic chuck 20 has only one electrode, the

distribution of the voltage potential on the electrostatic chuck 20 can be deemed uniform distribution and will not cause the aforementioned non-uniform distribution of the voltage potential difference between the plasma 16 and the electrostatic chuck 20. However, the electrostatic chuck 20 of the mono-polar type does not have a discharging circuit. When the HDPCVD process is over, the wafer 18 cannot be moved until the electric particles in the plasma 16 neutralize the inductive electric particles on the wafer 18. The neutralization process delays the throughput of mass production and if the wafer 18 is moved before the neutralization process is completed, the wafer 18 may be broken into fragments.

A bi-polar electrostatic chuck 201 is as shown in FIG.1B. If a bi-polar electrostatic chuck 201 is used in the HDPCVD process, after the HDPCVD process is over, the electrostatic force on the wafer 18 will be removed more rapidly by virtue of the discharging circuit created by the double electrodes. The discharging circuit created by the double electrodes can avoid delaying the throughput of mass production and prevent the wafer 18 from being broken into fragments. However, as shown in FIG.1C, the AC bias source 22 of producing ion-bombardment also connects to the inner electrode 28 and outer electrode 30 of the bi-polar electrostatic chuck 201 to produce the voltage potential difference between the plasma 16 and the bi-polar electrostatic chuck 201. Accordingly in the process of the transmission of high frequency AC currents, the inner electrode 28 power output always differs from the outer electrode 30 power output because of the impedance difference of the transmitting lines between the inner electrode 28 and the outer electrode 30 causing the non-uniform voltage potential distribution on

the bi-polar electrostatic chuck 201. As shown in FIG.2A, after ions bombard the inner side and outer side of the wafer 18, different voltage potential on the wafer 18 will be generated to produce surface currents on the wafer 18. As shown in FIG.2B, the surface currents on the wafer 18 will cause the accumulated electric particles on the conductive polysilicon layer 36. The gate oxide 38 on the silicon substrate 40 will be damaged by the accumulated electric particles passing through the gate oxide 38.

In order to solve the problem of the gate oxide damage, process steps are added to change the structure of the MOS device in the US. Pat. No. 5,913,140 and US. Pat. No. 5,843,827. However, the problem of the non-uniform voltage potential difference between the plasma 16 and the bi-polar electrostatic chuck 201 is not mentioned in these patents. Accordingly, how to avoid the non-uniform voltage potential difference between the plasma 16 and the bi-polar electrostatic chuck 201 is an important issue to be solved.

SUMMARY OF THE INVENTION

The main purpose of the present invention is to solve the aforementioned problem of the non-uniform voltage potential difference between the plasma and the bi-polar electrostatic chuck. The present invention provides a solution which adds an impedance-matching circuit between the AC bias power for generating the ion-bombardment and the bi-polar electrostatic chuck. The impedance-matching circuit can regulate the impedance of the inner electrode and the outer electrode of the bi-polar electrostatic chuck to balance the inner

electrode power output and the outer electrode power output. Furthermore, the impedance-matching circuit can lead to a uniform voltage potential difference between the plasma and the bi-polar electrostatic chuck to avoid the gate oxide damage caused by plasma. According to the experiment results, the fail rate of dies of a wafer decreases from 30%~60% without adding the impedance-matching circuit to 0%~2% with adding the impedance-matching circuit.

The impedance-matching circuit provided by the present invention includes a power-measuring device which can measure the voltage and the current of both the inner electrode and the outer electrode of the bi-polar electrostatic chuck and transform the voltage values and the current values into power output values of both the inner electrode and the outer electrode of the bi-polar electrostatic chuck, a power comparator which can compare the power value of the inner electrode and the power value of the outer electrode to get a control signal, and an automatic impedance-regulator which can receive the control signal to drive the logic drive motors to regulate the impedance values of the adjustable impedance-elements to let the inner electrode and the outer electrode of the bi-polar electrostatic chuck have the same power output.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIG.1A shows an illustrative chart of HDPCVD equipment of the prior art;

FIG.1B shows a top view of distribution of electric particles on a bi-polar electrostatic chuck of the prior art;

FIG.1C shows an equivalent circuit of the connection between an AC bias power for generating ion-bombardment and a DC(direct current) power for generating an electrostatic force on a bi-polar electrostatic chuck of the prior art;

FIG.2A shows surface currents on a wafer resulting from the power difference between the inner electrode and the outer electrode of a bi-polar electrostatic chuck of the prior art;

FIG.2B shows accumulated electric particles resulting from ion-bombardment on a conductive

poly-silicon layer passing through a gate oxide to damage the gate oxide of the prior art;

FIG.3A shows an illustrative chart of an inductively-coupled plasma reactor;

FIG.3B shows an equivalent circuit of the connection between an AC bias power for generating ion-bombardment and a DC(direct current) power for generating an electrostatic force on a bi-polar electrostatic chuck after adding an impedance-matching circuit;

FIG.3C shows the equivalent circuit of an impedance-matching circuit; and

FIG.4 shows a flow chart of adjusting impedance values of both the inner electrode and the outer electrode of a bi-polar electrostatic chuck.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Some embodiments of the invention will be described exquisitely as below. Besides, the invention can also be practiced extensively in other embodiments. That is to say, the scope of the invention should not be restricted by the proposed embodiments. The scope of the invention should be based on the claims proposed later.

As shown in FIG.3A, the apparatus capable of adaptive impedance matching of the present invention mainly applies to HDPCVD equipment. The HDPCVD equipment of the present invention is an inductively-coupled plasma reactor 101. The plasma 16 of high density and low energy is generated by an electromagnetic field produced by AC currents from an AC plasma generating power 12 passing through the inductive coils 14. In the preferred embodiment, the operating frequency of the AC plasma generating power 12 is nearly between 200KHz and 350KHz.

In HDPCVD process(such as the deposition of inter-metal dielectrics), before proceeding with the deposition of dielectrics, a wafer 18 desired to be deposited has to be secured onto a bi-polar electrostatic chuck 201. The bi-polar electrostatic chuck 201 is connected to a DC power 24 to produce an electrostatic force to secure the wafer 18 onto the bi-polar electrostatic chuck 201. After the HDPCVD process is over, the bi-polar electrostatic chuck 201 can provide a discharging circuit to remove the electrostatic force more rapidly than a mono-polar electrostatic chuck does to move the wafer 18 out of the inductively-coupled plasma reactor 101.

Depositing dielectric materials into gaps of high aspect ratio in a dielectric layer always leads to incomplete deposition and voids in the dielectric layer. The problem can be solved by means of both chemical vapor deposition process and anisotropic etching process of ion-bombardment of the HDPCVD process. In the present invention, the ion-bombardment results from an AC bias power 22. The AC bias power

22 connects to the bi-polar electrostatic chuck 201 for supporting the wafer 18. Then a DC self bias will be generated because of the surface area difference between the bi-polar electrostatic chuck 201 and the inductively-coupled plasma reactor 101. The generated DC self bias will attract ions in the plasma 16 to bombard onto the surface of the wafer 18 to etch excess deposited materials which stop following deposition. Further, a void-free deposition layer will be formed. The operating frequency of the AC bias power is about 13.56 MHz.

As shown in FIG.3B, the bi-polar electrostatic chuck has an inner electrode 28 and an outer electrode 30. The inner electrode 28 and the outer electrode 30 both connects to the DC power 24 and the AC bias power 22. The capacitive impedance for isolation of the inner electrode 321 and the capacitive impedance for isolation of the outer electrode 322 are used to prevent direct currents from entering the AC bias power 22 because capacitors to direct currents are open-circuit (capactive impedance $Zc = 1/j\omega C$, the frequency of direct current $\omega=0$, $Zc=\infty$).

The capacitive impedance for isolation of the inner electrode 321 and the capacitive impedance for isolation of the outer electrode 322 have different impedance values because of different transmitting lines. The different impedance values will lead to the power outputs difference between the inner electrode 28 and the outer electrode 30 (the power of AC bias power 22 $P_{generator}$ minus the power of the consumption of the impedance $P_{impedance}$ equals to power output P_{out}). In this situation when proceeding with ion-bombardment onto the wafer 18, surface currents will be generated. Surface currents on the wafer 18 will damage the gate oxides of the devices on the wafer 18. To avoid damaging the gate oxides

of the devices on the wafer 18, the inner electrode 28 power output and the outer electrode 30 of the bi-polar electrostatic chuck 201 power output should be the same. That is to say the impedance of the inner electrode 28 and the impedance of the inner electrode 30 have the same impedance values. To achieve this goal, an impedance matching circuit 42 is added in the present invention connecting the AC bias power 22 to the capacitive impedance for isolation of the inner electrode 321 and the capacitive impedance for isolation of the outer electrode 322 to let the capacitive impedance for isolation of the inner electrode 321 and the capacitive impedance for isolation of the outer electrode 322 have the same impedance values. And then the inner electrode power output will be the same with the outer electrode power output to avoid damaging gate oxides of the devices on the wafer 18.

One preferred embodiment of the present invention is as shown in FIG.3C, the impedance matching circuit mainly includes an adjustable capacitor of the inner electrode 441, an adjustable capacitor of the outer electrode 442, an adjustable inductor of the inner electrode 461, an adjustable inductor of the outer electrode 462, a power-measuring device 50, a power comparator 51, and an automatic impedance-regulator 52. One terminal of the impedance matching circuit 42 connects to the AC bias power 22 and the other terminal of the impedance matching circuit 42 connects to both the capacitive impedance for isolation of the inner electrode 321 and the capacitive impedance for isolation of the outer electrode 322.

The way of impedance-matching provided by the present invention includes the following steps: as shown by the power-

measuring block 500 in FIG.4 a power-measuring device 50 which can measure the voltage and the current of both the inner electrode 28 and the outer electrode 30 of the bi-polar electrostatic chuck 201 and transform the voltage values and the current values into power output values of the inner electrode 28 and the outer electrode 30 of the bi-polar electrostatic chuck 201, as shown by the power-comparing block 510 a power comparator 51 which can compare the power value of the inner electrode 28 and the power value of the outer electrode 30 to get a control signal, as shown by the automatic impedance-matching block 520, and an automatic impedance-regulator 52 which can receive the control signal to drive the logic drive motors to regulate the impedance values of the adjustable impedance-elements to let the inner electrode 28 and the outer electrode 30 of the bi-polar electrostatic chuck 201 have the same power output. Proceeding with the HDPCVD process at this time will not produce the voltage potential difference between the inner portion and the outer portion of the wafer 18 when the wafer 18 are bombarded by a plurality of ions because the inner electrode 28 power output is the same with the outer electrode 30 power output.

What is said above is only a preferred embodiment of the invention, which is not to be used to limit the claims of the invention; any change of equal effect or modifications that do not depart from the essence displayed by the invention should be limited in what is claimed in the following.